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Figure 6C (or Table 1) -8- Figs. 4-6B.

[0041] Table 1 shows the logic of the device select circuit in Figs. 4-6.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0042] A typical computer system in which the various aspects of the present invention are incorporated is illustrated generally in Fig. 1A. A typical computer system 101 has an architecture that includes a microprocessor 121 connected to a system bus 123, along with random access, main system memory 125 (which may include read only memory (ROM) and random access memory (RAM)), and at least one or more input-output (I/O) devices 127, such as a keyboard, monitor, modem and the like. Another main computer system component that is connected to a typical computer system bus 123 is a large amount of long-term, nonvolatile memory 129. Conventionally, such a mass storage is a disk drive with a capacity of tens of megabytes of data storage. During the functioning of the computer system 101, data from this mass storage 129 is retrieved into the system volatile RAM of main system memory 125 for processing, and new or updated data can be easily written back to the mass storage.

[0043] One aspect of the present invention is the substitution of a specific type of semiconductor memory system for the disk drive but without having to sacrifice non-volatility, ease of erasing and rewriting data into the memory, speed of access, and reliability. This is accomplished by employing an array of non-volatile, solid-state memory, integrated circuit chips. This type of memory has additional advantages of requiring less power to operate, and of being lighter in weight than a hard disk drive memory, thereby being especially suited for battery-operated portable computers.

[0044] The integrated circuit mass storage memory 129 includes one or more solid-state memory modules such as 131, 132 under the control of a controller module 133. Addresses, data, and commands are communicated between the memory modules 131, 132 and the controller module 133 by means of a device bus 135. The one or more memory modules such as 131, 132 can be selectively enabled by individual module select signals such as MS1*, MS2*. These signals are carried in select lines such as 151, 152 from the controller module to